## *Remarks*

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing Amendments, claims 1-20 are pending in the application, while claims 1-3, 6-13 and 18-20 were not elected under the restriction requirement. Among claims 4, 5 and 14-17 being considered in this reply, claims 4 and 14 are independent claims.

The Specification has been amended to correct minor grammatical errors and to make it consistent with the drawings. These amendments are fully supported by the specification as filed and no new matter is believed to be added. The entry of Amendments is respectfully requested.

Attached hereto is a marked-up version of the changes made by the current Amendment. The attachment is captioned "**Version with Markings to Show Changes Made.**"

***Rejections Under 35 U.S.C. § 112***

The Examiner rejected claims 4, 16 and 17 under 35 U.S.C. §112 for minor informalities. These amendments correct these informalities and the rejection under 35 U.S.C. §112 should now be withdrawn.

***Rejection Under 35 U.S.C. § 103***

On page 3 of the Office Action, the Examiner rejected claim 4 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,043,859 issued to Maeda ("Maeda").

Amended claim 4 recites a wire for a liquid crystal display, comprising: a wire layer made of either molybdenum or molybdenum alloy; a supplementary layer located either on or under said entire wire layer and made of either molybdenum nitride or molybdenum alloy nitride.

Neither Maeda nor the combination of alleged obviousness reference discloses nor suggests such new features. Therefore, claim 4 is patentable over Maeda. Likewise, claim 5 is also patentable over Maeda and the alleged obviousness reference.

On page 3, the Examiner rejected claim 5 under 35 U.S.C. §103(a) as being unpatentable over Maeda in view of U.S. Patent No. 6,011,277 issued to Yamazaki ("Yamazaki").

However, claim 5 is now dependent from claim 4 that is patentable over Maeda. Therefore, claim 5 is also patentable over Maeda. Since claim 5 is patentable over the primary reference, it may not seem necessary to consider the secondary reference, Yamazaki.

Thus, it is respectfully requested that all the outstanding objections and rejections over claims 4 and 5 be withdrawn and pass those claims to allowance.

On page 4, the Examiner rejected claim 14 under 35 U.S.C. §103(a) as being unpatentable over alleged prior art, in view of Maeda.

Amended claim 14 recites a liquid crystal display, comprising a supplementary data wire located either on or under the entire data wire and made of either molybdenum nitride or molybdenum alloy nitride.

Neither the alleged prior art nor the combination with Maeda discloses nor suggests such new features. Therefore, amended claim 14 is patentable over the alleged prior art and Maeda. Likewise, claims 15-17 that are dependent from the amended claim 14 are also patentable over the alleged prior art and Maeda.

On page 5, the Examiner rejected claims 15-17 under 35 U.S.C. §103(a) as being unpatentable over alleged prior art and Maeda, in further view of U.S. Patent No. 6,011,277 issued to Yamazaki ("Yamazaki").

However, as discussed previously, claims 15-17 are dependent from claim 14 that is patentable over the alleged prior art and Maeda. Therefore, claims 15-17 are also patentable over the alleged prior art and Maeda. Since claims 15-17 are patentable over the primary references, it may be no longer necessary to further consider the secondary reference, Yamazaki.

As such, it is submitted that the invention recited in claims 4, 5 and 14-17 are patentable over all the references of the record. A withdrawal of the outstanding rejections and issuance of claims 4, 5 and 14-17 are therefore respectfully requested.

## *Conclusion*

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete response has been made to the outstanding Office Action and, as such, the present application with claims 4, 5 and 14-17 is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

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Date: 14 MAY 01

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## Version with Markings to Show Changes Made

***Amendments***

***In the Specification***

Please enter the following amendments:

Page 1, line 24, change "for" into – to form –:

To manufacture the liquid crystal display, deposition, photolithography and etch steps are required [for] to form the gate wire, the data wire, the gate insulating layer, the passivation layer and the pixel electrodes.

Page 2, line 4, change "vapor phase" into – vaporized –.

There are two general methods for depositing a thin film, a chemical vapor deposition (CVD) and a physical deposition. The CVD forms the film by the reaction of [vapor phase] vaporized chemicals that contain the required constituents, while a sputtering which is a kind of physical deposition obtains the film by having energetic particles to strike target to be sputtered physically. The CVD is generally used to form the semiconductor layer and insulating layers such as the gate insulating layer and the passivation layer, and the sputtering is used to form metal layers for the gate wire and the data wire and an ITO layer for the pixel electrodes.

Page 3, line 7, after "have" insert – a –.
Page 3, line 8, change "disconnections of the wires" into – chances of wire disconnection –.

Because the wires according to the present invention have a low etch rate for the

ITO etchant including strong acid, the [disconnections of the wires] chances of wire disconnection are reduced.

Page 5, line 11, change "220" into – 210 –.

A gate insulating layer 300 covers the gate wire 200, 210 and 230, a hydrogenated amorphous silicon (a-si:H) layer 400 and a doped hydrogenated amorphous silicon layer 410 and 420 including N type impurity are sequentially formed on the gate insulating layer 300 opposite the gate electrode 210, and the portions 410 and 420 of the doped amorphous silicon layer are opposite each other with respect the gate electrode [220]210.

Page 5, line 21, change "530" into – 520 –.

A supplementary data wire 550 made of either molybdenum nitride or molybdenum alloy nitride is formed under the data wire 500, 510 and [530]520. The molybdenum alloy used in this embodiment comprises one selected from tungsten, chromium, zirconium, and nickel of the content of 0.1 to less than 20 atm %. The supplementary data wire 550 may be located on the data line 500.

Page 6, line 2, change "700" into – 600 –.
Page 6, line 4, change "700" into – 600 –.
Page 6, line 10, change "700" into – 600 –.
Page 6, line 11, change "720" into – C2 –.
Page 6, line 12, after "characteristics" insert – is –.
Page 6, line 12, change "700" into – 600 –.

A passivation layer [700]600 is formed on the data wire 500, 510 and 520 and portions of the amorphous silicon layer 400 which is not covered by the data wire 500, 510 and 520. The passivation layer [700]600 has a contact hole C1 exposing the drain

electrode 520, and another contact hole C2 exposing the gate pad 230 along with the gate insulating layer 300. Here, the description of a data pad connected to the data line 500 is omitted.

Finally, a pixel electrode 700 formed of ITO (indium tin oxide) and connected to the drain electrode 520 through a contact hole C1 is formed on the passivation layer [700]600. Furthermore, a gate ITO layer 710 that connects to the gate pad 230 through the contact hole [720]C2 and improves the contact characteristic[s] is formed on the passivation layer [700]600.

Page 6, line 17, after "according" insert – to –.

Figs. 4A-4F show cross sectional views of the intermediate structures of the TFT array panel shown in Fig. 1 to Fig. 3 manufactured by a manufacturing method according to the embodiment of the present invention.

Page 7, lines 1-2, change "equal to or more than 0.5 times that of argon gas" into – no smaller than a half of argon gas –.

As shown in Fig. 4A, a nitride layer 251 made of either molybdenum nitride or molybdenum alloy nitride is deposited on a transparent insulating substrate 100 by using a reactive sputtering method. The target for the reactive sputtering is made of either molybdenum and molybdenum alloy having one selected from tungsten, chromium, zirconium, and nickel of the content ratio of 0.1 to less than 20 atm %. A reactive gas mixture includes argon gas (Ar) and nitrogen gas ($N_2$), and the inflow amount of the nitrogen gas is [equal to or more than 0.5 times that of argon gas]no smaller than a half of argon gas. Thereafter, a metal layer 201 made of either molybdenum or molybdenum

alloy is deposited by sputtering. The metal layer 201 may be deposited before the deposition of the nitride layer 251.

Page 7, line 23, change "is deteriorates" into – affects –.

As shown in Fig. 4C, a gate insulating layer 300 made from silicon nitride, a hydrogenated amorphous silicon layer and an extrinsic or doped hydrogenated amorphous silicon layer highly doped with N type impurity are sequentially deposited by plasma-enhanced chemical vapor deposition (PECVD hereafter). The amorphous silicon layer and the extrinsic amorphous silicon layer are patterned by photolithography to form an active pattern 401 and 411. A nitride layer 551 made of either molybdenum nitride or molybdenum alloy nitride with the thickness of 300~1,000 Å is deposited by using reactive sputtering method, and a metal layer 501 made of either molybdenum or molybdenum alloy with the thickness of 1,000 - 4,000 Å is deposited. The metal layer 501 may be deposited before the deposition of the nitride layer 551. When the thickness of the nitride layer 551 is less than 300 Å, it is difficult to obtain the uniform thickness, and the thickness of more than 1,000 Å [is deteriorates]affects the following etch step.

Page 8, line 6, change "larger" into – higher –.

As shown in Fig. 4D, the metal layer 501 and the nitride layer 551 are sequentially patterned to form a data wire including a data line 500, a source electrode 510, a drain electrode 520, a data pad (not shown), and a supplementary wire 550 by performing wet-etch using the above-described aluminum etchant. Because the etch rate for the upper metal layer 501 is [larger]higher than the etch rate for the low nitride layer 551, the metal

layer 501 may be over-etched. Accordingly, it is desirable that the thickness of the nitride layer 551 is less than 1,000 Å to prevent the over-etch of the metal layer 501.

Page 8, lines 9-12, please amend the paragraph as follows:

Thereafter, exposed portions of the doped [extrinsic] amorphous silicon layer 411 is removed to divide [such that] the doped [extrinsic] amorphous silicon layer into [is then divided] two portions of 410 and 420, and the central portion of the amorphous silicon layer 400 is exposed.

Page 8, line 19, change "720" into – C2 –.

Finally, an ITO layer is deposited and patterned to form a pixel electrode 700 connected to the drain electrode 520 through the contact hole C1 and a gate ITO layer 710 connected to the gate pad 230 through the contact hole [720] C2 as shown in Fig. 4F. Here, the etchant for the ITO layer comprises hydrochloric acid and nitric acid, which may penetrate along the crack of the passivation layer 600 or along the edges of the ITO wire 700 and 710, and then may reach the data wire 500, 510 and 520, and the gate pad 230.

Page 9, line 1, change "reactivation" into – reaction –.

However, because the supplementary gate wire 250 and the supplementary data wire 550 have a low chemical reaction [reactivation] against the ITO etchant, the gate wire 200, 210 and 230, and the data wire 500, 510 and 520 through the supplementary gate wire 250 and the supplementary data wire 550 are not disconnected.

Page 9, line 7, change "reactivation" into – reaction –.

Next, the etch rate of a molybdenum-tungsten alloy nitride layer as function of volume of nitrogen gas as a reactive gas for aluminum and ITO etchants is described to confirm the low chemical reaction [reactivation] of the supplementary gate and data wires 250 and 550 for aluminum and ITO etchants.

***In the Claims:***

Please amend claims 4, 14, 16 and 17 as follows:

4. (Amended) A wire for a [display] liquid crystal display, comprising:

a wire [main] layer made of either molybdenum or molybdenum alloy;

a supplementary layer [which is] located either on or under said entire wire [the main] layer and made of either molybdenum nitride or molybdenum alloy nitride.

14. (Amended) A [display] liquid crystal display, comprising:

an insulating substrate;

a gate wire formed on the substrate;

a gate insulating layer covering the gate wire;

a data wire [which is] made of one of either molybdenum or molybdenum alloy and formed on the gate insulating layer;

a supplementary data wire [which is]located either on or under the entire data wire and made of either molybdenum nitride or molybdenum alloy nitride;

a passivation layer formed on the data wire or the supplementary data wire; and

an ITO pixel electrode formed on the passivation layer and connected to the data wire through a contact hole formed in the passivation layer.

16. (Amended) The liquid crystal display of 15[17], further comprising:

a supplementary gate wire which is located either on or under the gate wire and made of either molybdenum nitride or molybdenum alloy nitride.

17. (Amended) The liquid crystal display of claim 16[18], wherein the supplementary gate wire comprises one selected from the group consisting of tungsten, chromium, zirconium and nickel.